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(54) Title: COPPER-INDIUM BASED THIN FILM PHOTOVOLTAIC DEVICES AND METHODS OF MAKING THE SAME

Example	Window	Window Dopant	Absorber Layer 1	Absorber Layer 2	Absorber Layer 3	Back Contact	Treatment
I Figs 2-4	n-type ZnSe; CdS; or Cu$_2$O;	group III or VII Element	n-type	n-type	N/A	n-Schottky	Chemically treat, anneal, etch device as appropriate;
II Figs 5-7	n-type ZnSe; CdS; or Cu$_2$O;	group III or VII Element	n-type	p-type	N/A	p-Ohmic	Chemically treat, anneal, etch device as appropriate;
III Figs 8-10	n-type ZnSe; CdS; or Cu$_2$O;	group III or VII Element	n-type	p-type	p-type	p-Ohmic	Chemically treat, anneal, etch device as appropriate;
IV Figs 11-13	p-type ZnSe;	group I or V Element	p-type (doped)	n-type (doped)	N/A	n-Ohmic	Chemically treat, anneal, etch device as appropriate;

(57) Abstract: A method of fabricating a copper-indium based thin film photovoltaic device comprises the steps of: (a) using electrodeposition, depositing a front window layer of a semiconductor material on a suitably configured electrically conductive substrate; (b) doping the window layer to obtain optimum electrical conductivity in the window layer; and following steps (a) and (b), (c) successively electrochemically depositing a plurality of adjacent copper-indium based semiconductor absorber layers on the window layer wherein each absorber layer has a different band gap energy value to an adjacent absorber layer. Thus a copper-indium based thin film photovoltaic device made according to this method comprises; an electrically conductive front substrate upon which is comprised an electrodeposited window layer of a doped semiconductor material; and having been successively deposited on top of said deposited window layer, a plurality of electrochemically deposited adjacent copper-indium based semiconductor absorber layers, wherein each absorber layer has a different band gap energy value to an adjacent absorber layer.

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COPPER-INDIUM BASED THIN FILM PHOTOVOLTAIC DEVICES AND METHODS OF MAKING THE SAME

Field of the Invention

The present invention relates to the field of thin film photovoltaic devices which comprise copper-indium based semi-conducting materials such as, for example, copper-indium disulfide ($CuInS_2$), copper-indium dieseling ($CuInSe_2$) or copper-indium ditelluride ($CInTe_2$) based materials. The invention relates to improved methods of making such devices in addition to achieving high efficiency devices themselves.

Background to the Invention

Photovoltaic cells and methods of their production are relatively advanced in the field of crystalline silicon cells. However, thin film technology is known to hold the promise of reducing costs of solar cell manufacture through substantial reducing the quantity of semi-conductor materials and energy used during production. Thus, there is a general trend towards the use of thin film solar cells so as to reduce solar cell module costs. Various types of clearly distinct thin film photovoltaic cells have emerged, these being the multi-crystalline silicon cell, the amorphous silicon cell, the cadmium telluride/cadmium sulphide hetero-junction cell and the copper-indium diselenide based/cadmium sulphide hetero-junction cell, the latter being the subject of an aspect of the present invention.

A known prior art structure of a copper-indium dieseling based solar cell 101 is schematically illustrated in Fig. 1 and comprises a metal back contact 102 (usually a molybdenum (Mo) layer evaporated on a glass substrate) configured to be able to enable the layer to be connected into an external electrical circuit, a copper-indium diselenide absorber layer 103 deposited upon metal back contact

layer 102, a cadmium sulphide or zinc oxide n-type window layer 104 deposited upon layer 103 and a transparent front electrical contact layer (or any other metal grid) 105 deposited upon layer 104 to complete the device.

Various prior art methods of making such a device are known by those skilled in the art including selenisation whereby hydrogen selenide gas is passed over the surface of an indium/copper layer at about 400°C. However, various problems result in such techniques such as large stresses being induced in the copper-indium deselenide based film. Prior art methods have, to some extent, overcome fabrication problems, but are still somewhat complicated in view of the use of sputtering of copper and indium and various difficulties surrounding satisfactory substrate preparation. However, problems in respect of adherence of the copper-indium diselenide based film to the device would still benefit from significant improvement. Commercially available large area copper-indium diselenide based solar panels generally have efficiencies of around 8% with the devices being stable over periods of several years. To improve efficiency further there is a need to improve uniformity of deposition of the copper-indium diselenide based and other layers and there is some belief in the industry that large area solar panel having efficiencies of around 12-14% will be available in the next few years, particularly through use of copper-indium/gallium diselenide (CIGS) technology.

Thin films of copper-indium diselenide based materials, for example, have been produced using a variety of deposition techniques such as elemental co-evaporation, sputtering, pulsed laser deposition and electrodeposition. Electrodeposition is a low cost technique suitable for fabrication of large area photovoltaic devices with scaling capability to produce solar modules of commercially viable dimensions. Thin film photovoltaic devices based on electrodeposition followed by evaporation and selenisation of $CuInSe_2$ have reached efficiencies of 9.4% to date for lab scale devices as reported by R. N. Bhattacharya et al., J. Electrochemical Soc. Vol. 143, No. 3 (1996), p.854. Electrodeposition and evaporation and selenisation of CIGS have produced even

higher efficiencies of 14.1% to date for small-scale devices as reported by R.N. Bhattacharya et al., J. Electrochem. Soc., Vol. 145, No. 10, (1998), p. 3435. The highest reported efficiency for small scale photovoltaic devices produced from expensive materials growth techniques, for example elemental co-evaporation, is around 18.8% as reported by M.A. Contreras et al., Prog. Photovolt. Res. Appl. 7, (1999), p. 311.

To achieve low cost and higher efficiencies which are attractive for commercialization of photovoltaic cells in solar power generation, the electrodeposition method and processing steps involved in copper-indium based semi-conductor device fabrication requires improvement and, in particular, there is a need to improve one step electro-deposition of the copper-indium based material on glass/transparent conducting oxide (TCO) substrates.

Many prior art copper-indium based photovoltaic device configurations and methods of making photovoltaic devices are known. Canadian patent no. CA 2056609 discloses electrodeposition of a plurality of copper-indium based layers in a given order. However, although functional devices result from the methods disclosed in CA 2056609 the efficiency of the resulting devices may be considered to leave considerable room for improvement.

In view of the above there is clearly a need to improve efficiency and cut down production costs of copper-indium based photovoltaic solar cells. To improve efficiency both new and improved low cost techniques of fabrication are required so that a greater proportion of electromagnetic radiation is converted into useful electrical power. Additionally, existing devices generally degrade with time and there is a desire to create new copper-indium based photovoltaic cell designs so that the resultant devices may effectively improve in efficiency over time rather than degrade. For commercial viability it is generally a requirement that a given photovoltaic panel should exhibit over 15% efficiency and utilize minimal materials and minimize other detrimental factors associated with many existing technologies.

Summary of the Invention

An object of the present invention is to reduce costs associated with manufacturing thin film copper-indium based photovoltaic devices. This object is achieved by reducing the amount of materials required for construction of copper-indium based photovoltaic devices and solar cells and by using a low cost electrodeposition technique to successfully deposit copper-indium based semi-conducting materials.

A further objective of the present invention is to design and manufacture multi-layer graded band gap photovoltaic devices to capture a major part of the solar spectrum and hence to maximize efficiency. This object can be achieved, at least in part, by one or more of the following:

stacking different semiconductor layers so that internal electric fields at each junction add up to form an effective tandem solar cell;

allowing the semiconductor materials to alloy at hetero-junctions to form smooth and graded band gaps during annealing and aging processes to improve the conversion to useful electrical power of a major part of the solar spectrum and also to improve the charge carrier collections;

enabling semiconductor layers to be produced by simply changing the stoichiometry of the materials by varying the deposition voltages; and

enabling thin film copper-indium based semiconductor layers to be grown with improved grain formation with appropriate doping so as to maximize the conversion efficiency of photovoltaic devices.

A further object of the present invention is to manufacture photovoltaic devices including solar cells which improve the structural requirements at hetero-junctions and hence device efficiency with age and with heat-treatment.

Yet a further object of the present invention is to enable the profitable manufacture of high efficiency photovoltaic devices and solar cells to be realized such that the efficiency achieved is over 15% and a minimal amount of semiconductor material is used (of the order of two microns thick), this being achieved using a relatively inexpensive electrodeposition technique.

According to a first aspect of the present invention there is provided a method of fabricating a substantially copper-indium based thin film photovoltaic device, said method being characterised by comprising the steps of:

(a) using electrodeposition, depositing a front window layer of a semiconductor material on a suitably configured electrically conductive substrate;

(b) doping said window layer to obtain optimum electrical conductivity in said window layer; and following steps (a) and (b),

(c) successively and electrochemically depositing a plurality of adjacent copper-indium based semiconductor absorber layers on top of said semiconductor window layer wherein each said absorber layer has a different band gap energy value to an adjacent said absorber layer.

Preferably said adjacent copper-indium based semiconductor absorber layers are selected from the set of compounds comprising:

copper-indium disulphide based compounds;

copper-indium diselenide based compounds; and

copper-indium ditelluride based compounds.

Preferably the method additionally comprises the step of:

treating the outer surface of each absorber layer to optimise the electrical properties of said outer semiconductor absorber layer.

Preferably said treatment comprises chemically etching said outer semiconductor absorber layer.

Preferably the method additionally comprises the step of:

metalising the outer surface of said outer semiconductor absorber layer so as to enable said device to be connectable to an electric circuit.

Preferably said method comprises the additional step of annealing said semiconductor layers at a temperature in the temperature range 325-375°C and preferable the annealing step is completed before the etching and metalisation steps.

Preferably said window semiconductor layer comprises:

an n-type semiconductor material selected from the set comprising ZnSe, CdS and Cu_2O.

Preferably said window dopant is selected from the set of dopants comprising Group III; and Group VII elements.

Preferably said window layer comprises a p-type semiconductor material.

Preferably said window layer comprises a p-type ZnSe semiconductor material.

Preferably said window semiconductor layer is doped with a dopant selected from the set of dopants comprising:

Group I; and Group V elements.

Preferably said window layer has a greater band gap energy value than any of said plurality of absorber layers.

Preferably the band gap energy value of said absorber layers decreases with increased distance of a given said layer away from said window layer.

Preferably a first deposited absorber layer comprises an n-type semiconductor material; and

a second absorber layer deposited adjacent to said first absorber layer comprises an n-type semiconductor material.

Preferably said device further comprises a back Schottky barrier metal electrical contact layer adjacent to the outermost deposited absorber layer.

Preferably a first said deposited absorber layer comprises an n-type semiconductor material; and

a second said absorber layer deposited adjacent to said first absorber layer comprises a p-type semiconductor material.

Preferably a first said deposited absorber layer comprises an n-type semiconductor material; a second said deposited absorber layer adjacent to said first absorber layer comprises a p-type semiconductor material; and an outer absorber layer adjacent to said second absorber layer comprises a close to p-type semiconductor material.

Preferably said device comprises a back Ohmic type electrical contact layer adjacent to the outermost deposited close to p-type absorber layer.

Preferably a first said deposited semiconductor absorber layer comprises a p-type semiconductor material; and

a second said deposited semiconductor absorber layer, adjacent to said first said absorber layer, and comprises an n-type semiconductor material.

Preferably said device further comprises:

a back Ohmic type electrical contact layer adjacent to said second said deposited n-type absorber layer.

According to a second aspect of the present invention there is provided a substantially copper-indium based thin film photovoltaic device, wherein said device is characterised in that it comprises:

an electrically conductive front substrate upon which is comprised an electrodeposited window layer of a doped semiconductor material; and

having been successively deposited on top of said deposited window layer, a plurality of electrochemically and adjacently deposited copper-indium based semiconductor absorber layers, wherein each said absorber layer has a different band gap energy value to an adjacent absorber layer.

Preferably said adjacent copper-indium based semiconductor absorber layers comprise at least one compound from the set comprising:

Cooper-indium disulphide based compounds;

copper-indium diselenide based compounds; and

copper-indium ditelluride based compounds.

Preferably the outer surface of each absorber layer has been treated by chemical treatment, annealing and etching to optimise the electrical properties of said outer semiconductor absorber layers.

Preferably said absorber layers have been chemically treated and annealed using a suitable doping agent such as indium trichloride ($InCl_3$) to improve n-type conduction.

Preferably said window layer comprises a material from the set comprising:

n-type ZnSe; n-type CdS; and n-type Cu_2O.

Preferably said dopant comprises an element to improve n-type conduction, said element being selected from the set comprising:

Group III elements; and Group VII elements.

Preferably said window material comprises a p-type semiconductor material.

Preferably said window material comprises p-type ZnSe based material.

Preferably said window material is doped with an element to improve p-type conduction, said element being selected from the set comprising:

Group I elements; and Group V elements.

Preferably said window layer has a greater band gap energy value than the band gap value of any of said plurality of absorber layers.

Preferably the band gap energy value of said absorber layers decreases with increased distance of a given said absorber layer away from said window layer.

Preferably said first said deposited absorber layer, deposited adjacent to said window layer, comprises an n-type semiconductor material; and

a second absorber layer deposited adjacent to said first absorber layer comprises an n-type semiconductor material.

Preferably said device further comprises a back Schottky barrier metal contact layer adjacent to the outermost deposited absorber layer.

Preferably a first said deposited absorber layer comprises an n-type semiconductor material: and

a second said absorber layer deposited adjacent to said first absorber layer comprises of p-type semiconductor material.

Preferably the first said deposited absorber layer comprises an n-type semiconductor material; a second said deposited absorber layer adjacent to said first absorber layer comprises a close to p-type semiconductor material; and an outer absorber layer adjacent to said second absorber layer comprises a p-type semiconductor material.

Preferably said device comprises a back Ohmic electrical contact layer adjacent to the outermost deposited p-type absorber layer.

Preferably a first said deposited absorber layer comprises a p-type semiconductor material; and

a second said deposited absorber layer, adjacent to said first deposited absorber layer, comprises an n-type semiconductor material.

Preferably said device comprises a back Ohmic electrical contact layer adjacent to said second deposited n-type absorber layer.

Preferably said device, comprises n-type window material and during operation, conducts electric current in accordance with:

electrons move substantially from said absorber layers to said window layer; and

holes move in the opposite direction to said electrons.

Alternatively, preferably said device comprises p-type window material and during operation conducts electrical current in accordance with:

electrons move in a direction towards an Ohmic contact from said window layer through said respective absorber layers, each said respective absorber layer having a smaller band gap than the last; and

holes move substantially in the opposite direction to said electrons.

According to a third aspect of the present invention, there is provided a method of fabricating a substantially copper-indium based thin film photovoltaic device of the type comprising:

a deposited n-type or p-type window layer of a semiconductor photon absorber material; and

at least a first deposited substantially copper-indium based photon absorber layer located substantially adjacent to said window layer;

said method being characterised by comprising the step of:

doping said first photon absorber layer with a dopant of the same type, that is n-type or p-type, as said window layer.

Preferably said first deposited copper-indium based layer is assumed to be of the same type (p-type or n-type) as said window layer.

Preferably said selected window material is n-type and said first photon absorber layer is doped with an n-type dopant.

Preferably said n-type window layer is doped with an n-type dopant.

Preferably said window layer is doped with a group III or VII element.

Preferably said selected window layer is n-type doped with a group III or VII element and said first absorber layer is n-type, said method additionally comprising the steps of:

depositing a second n-type substantially copper-indium based photon absorber layer adjacent to said first copper-indium based photon absorber layer; and configuring a back electrical contact to said second photon absorber layer wherein said back contact constitutes an n-Shottky type barrier.

Preferably said selected window layer is n-type doped with a group III or VII element and said first photon absorber layer is n-type, said method additionally comprising the steps of:

depositing a second substantially copper-indium based photon absorber layer adjacent to said first photon absorber layer said second photon absorber layer being substantially p-type; and

configuring a back electrical contact to said second photon absorber layer wherein said back contact constitutes a p-Ohmic type contact.

Preferably said selected window layer is n-type doped with a group III or VII element and said first absorber layer is n-type, said method additionally comprising the steps of:

depositing a second substantially copper-indium based photon absorber layer adjacent to said first photon absorber layer, said second photonabsorber layer being substantially p-type;

depositing a third substantially copper-indium based photon absorber layer adjacent to said second photon absorber layer, said third photonabsorber layer being substantially p-type; and

configuring a back electrical contact to said third, that is the outer, photonabsorber layer wherein said back contact constitutes a p-type Ohmic contact.

Preferably said selected window material is p-type and said first photon absorber layer is doped with a p-type dopant.

Preferably said p-type window layer is doped with a p-type dopant.

Preferably said window layer is doped with a group I or V element.

Preferably said selected window layer is p-type doped with a group I or V element and said first photon absorber layer is p-type, said method additionally comprising the steps of:

depositing a second substantially copper-indium based photon absorber layer adjacent to said first photon absorber layer, said second photon absorber layer being substantially n-type; and

configuring a back electrical contact to said second photon absorber layer wherein said back contact constitutes an n-Ohmic type contact.

Preferably said window layer is deposited on a substrate and said first deposited substantially copper-indium based photon absorber layer is then deposited on said window layer.

Preferably, following the deposition of said first substantially copper-indium based photon absorber layer there are successfully deposited further layers of substantially copper-indium based photon absorber materials.

Preferably said deposition of said layers is by electrodeposition.

Preferably the order of deposition of the layers is:

the window layer followed by said first deposited copper-Indium based photon absorber layer followed, if applicable, by successive deposition thereafter of one or more further substantially copper-indium based photon absorber layers.

According to a fourth aspect of the present invention, there is provided a substantially copper-indium based thin film photovoltaic device of the type comprising:

an n-type or p-type window layer of a semiconductor photon absorber material deposited on an electrically conductive substrate; and

at least a first deposited substantially copper-indium based photon absorber layer located substantially adjacent to said window layer;

said device being characterised in that:

said first photon absorber layer has been doped with a dopant of the same type, that is n-type or p-type, as said window layer.

Preferably in such a thin film photovoltaic device said window layer has been deposited on a substrate and thereafter said first deposited substantially copper-indium based photon absorber layer has been deposited on said window layer.

Preferably the order of deposition of said layers is as follows:

the window layer followed by said first deposited copper-indium based photon absorber layer and tehn if appropriate, on top of said first photon absorber layer successive deposition thereafter of one or more further copper-indium based photon absorber layers.

Brief Description of the Drawings

For a better understanding of the invention and to show how the same may be carried into effect, there will now be described by way of example only, specific embodiments, methods and processes according to the present invention with reference to the accompanying drawings in which:

Fig. 1 schematically illustrates the structure of a typical prior art copper-indium diselenide photovoltaic cell;

Fig. 2 schematically illustrates the structure of a first example of a copper-indium based photovoltaic cell as configured in accordance with the present invention;

Fig. 3 details the energy band diagram of the device schematically illustrated in Fig. 2 and comprises a large Schottky contact at the junction between the back metal contact layer and adjacent absorber layer in addition to two hetero-junctions with enhancing internal electric fields;

Fig. 4 schematically illustrates steps involved in fabricating the device schematically illustrated in Fig. 2;

Fig. 5 schematically illustrates a second embodiment of a copper-indium based photovoltaic cell as configured in accordance with the present invention;

Fig. 6 shows the energy band diagram of the device schematically illustrated in Fig. 5;

Fig. 7 schematically illustrates the steps involved in fabricating a device of the type schematically illustrated in Fig. 5;

Fig. 8 schematically illustrates a third preferred embodiment of a copper-indium based photovoltaic cell as configured in accordance with the present invention;

Fig. 9 details the energy band diagram of the device illustrated in Fig. 8;

Fig. 10 schematically illustrates the steps involved in fabricating the device illustrated in Fig. 8;

Fig.11 illustrates schematically a fourth preferred embodiment of a copper-indium based photovoltaic cell as configured in accordance with the present invention;

Fig. 12 illustrates schematically the energy band diagram of the device illustrated schematically in Fig. 11;

Fig. 13 illustrates schematically the steps involved in fabricating the device illustrated in Figs. 11 and 12; and

Fig. 14 summarizes, in the form of a table, the devices as configured in accordance with the present invention and as described by way of example in figures 2 - 13.

Detailed Description of the Best Mode for Carrying Out the Invention

There will now be described by way of example the best mode contemplated by the inventors for carrying out the invention. In the following description numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent however, to one skilled in the art, that the present invention may be practiced without limitation to these specific details. In other instances, well known methods and structures have not been described in detail so as not to unnecessarily obscure the present invention.

Low cost and high efficiency solar cells and photovoltaic devices in general may be produced in accordance with the present invention using electrodeposition of the relevant semi-conducting layers. Various examples of multi-layer graded band gap photovoltaic cell structures are given below, each of which may use zinc selenide (ZnSe), cadmium sulphide, (CdS) or copper oxide (Cu_2O) layers as an n-type window material or p-type ZnSe window material. As illustrated in the following examples, ternary or quaternary compounds of $CuInS_2$, $CuInGaS_2$, $CuInSe_2$, $CuInGaSe_2$, $CuInTe_2$ or $CuInGaTe_2$ may be used as n-type or p-type absorber layers in a given device structure under fabrication. In each case a suitable back metal contact may, for example, be prepared by vacuum evaporation after heat treatment and surface preparation.

Semiconductor materials for use as absorber layers in a device fabricated in accordance with the present invention suitably include materials based on:

copper-indium disulphide ($CuInS_2$).

copper-indium diselenide ($CuInSe_2$); and

copper-indium ditelluride ($CuInTe_2$),

These materials may be represented by the generalised chemical formula:

$CuInX_2$

where X = S, Se or Te respectively.

Example 1

Fig. 2 schematically illustrates a first preferred embodiment of a multi-layer graded band gap photovoltaic device structure as configured in accordance with the present invention. The example given comprises an n-n-n-layer three junction device structure 201 with a large Schottky barrier at the back contact. The corresponding energy band diagram (not to scale) is schematically illustrated in Fig. 3. Device 201 comprises a glass substrate 202 as the holder to receive light, such as sunlight in the case of a solar cell. Adjacent to glass substrate 202 is a transparent conducting glass layer 203 configured for attachment to an electric circuit. Layer 203 may suitably comprise fluorine doped tin oxide (FTO) or indium doped tin oxide (ITO). Adjacent to layer 203 is configured a window material 204, such as n-ZnSe which has a band gap of 2.7 eV. Adjacent to window material 204 is a first absorber layer (n-type) 205 which may suitably comprise n-$CuInS_2$ for example which has a band gap of 1.5 eV. Adjacent to layer 205 is a second absorber layer 206 which may suitably be formed of n-type $CuInSe_2$ which has a band gap of 1.1 eV. Window material 204 may comprise ZnSe (2.7 eV), CdS (2.4 eV) or Cu_2O (2.2 eV) n-type materials, for example. The

energy band diagram of Fig. 3 in relation to the device of Fig. 2 clearly details the large Schottky barrier formed at the back between absorber layer 206 and the metal contact layer 207. The potential barrier height of the Schottky contact is given by Φ_b and this produces the highest internal electric field in the device. The large Schottky barrier 301 and the two hetero-junctions effectively provide an increased slope of energy band value which results in an increased electric field that facilitates flow of electric current through the device and through a circuit attached thereto. The gradient of the band energy curve 304 increases in a direction from the outer conducting glass layer 203 towards the Schottky barrier. The slope (gradient) is defined as the rate of change of the potential (V) with respect to distance (x) as is well known to those skilled in the art. Thus electric field strength E is given by the following formula:

$$E = -\frac{dV}{dx}$$

Therefore as is indicated in the diagram, electrons (e) 302 move respectively through absorber layers 206, 205 and window material 204 into the front contact, the transparent conducting glass layer (203). An increase in the gradient of curve 304 corresponds to an increase in the electric field strength E in accordance with the above equation. Similarly, holes (h) 303 are indicated as moving through window layer 204 and absorber layers , 205 and 206 into the back metal contact 207. Progressively, received sunlight is absorbed as it is transmitted through the device, the electromagnetic absorption varying throughout the device depending on the band gap of the layer in which the light is being transmitted. One example of such an n-n-n-layer device is:

Glass/CG/n-ZnSe/n-$CuInS_2$/n-$CuInGaSe_2$/large Schottky contact

Steps involved in producing the device identified in Fig. 2 are detailed in Fig. 4. At step 401 a glass/conducting glass substrate is cleaned to remove grease from the surface. Following step 401 at step 402 the prepared substrate is placed in a suitably configured electrodeposition chamber to enable deposition of an n-type window layer to be formed upon the glass/conducting glass substrate.

Suitable n-type window layers are as detailed above. Following step 402, at step 403 the glass substrate layer comprising the window layer is doped using a suitable Group III or Group VII element by chemical treating and annealing, so as to obtain optimum electrical conductivity. Following step 403 the resultant structure is further processed by chemical etching and electroplating to deposit an absorber layer onto the surface of the window layer processed at step 403. Following deposition of a given absorber layer, for example n-$CuInS_2$, at step 404, the electrodeposited absorber layer is doped to obtain optimum n-type conduction at step 405. At step 406, a question is asked as to whether any more absorber layers are required to be deposited. In accordance with the present invention one or more further layers will be deposited, the further absorber layers having respectively a lower band gap energy as further layers are deposited. If the question asked at step 407 is answered in the affirmative then a further absorber layer is deposited via electroplating, such as n-$CuInGaSe_2$ at step 404 and doping of the second absorber layer is undertaken at step 405 and the question asked at step 406 asked again. Steps 404 to 406 are repeated until no further absorber layers are required whence the resultant structure is further treated at step 407. At step 407 the final absorber layer electrodeposited at step 404 is heat treated and chemically etched so as to enhance electrical property and form a large Schottky barrier diode upon depositing a back metal electrical contact at step 408. Following the above steps, the final device structure is completed and ready for use.

Further details regarding electrodeposition of a given absorber layer are provided as follows by way of example. Electrodeposition of CIS has been carried out by the inventors using a standard three electrode set up using an EG & G Princeton Applied Research model 362 scanning protentiostat. The counter electrode was a carbon rod and the reference electrode used was Ag/AgCl. The working electrode, cathode, was a conducting glass (CG) coated glass substrate. Both indium doped tin oxide (ITO) and fluorine doped tin oxide (FTO) have been found to be particularly suitable materials for use as the CG.

Electrodeposition of $CuInSe_2$ films on CG coated glass substrates is readily carried out in an electro-chemical cell containing aqueous solution of $CuSO_4$, $In_2(SO_4)_3$ and SeO_2 in the ratio from 1:2:1 to 1:100:10. The pH of the electrolyte may suitably vary between around 2.50 and 2.90 without addition of any acid into the solution. It has been found that the addition of acid to the electrolyte has the disadvantageous effect of reducing adherence of the films to the CG substrate. The temperature of the electrolyte is preferably maintained at 60-65°C, because the inventors have observed that films grown at this temperature are more crystalline than those grown at room temperature. Those skilled in the art will therefore realize that this produces enhanced electrical properties as regards the efficiency of a given photovoltaic cell under construction. Furthermore, a slow stirring has been found to improve the quality of the films being made. Suitably the electrodeposition is carried out under potentiostatic conditions of deposition voltage which vary from -0.4V to -0.6V against the Ag/AgCl electrode. Prior to material deposition the transparent conducting glass (TCG) substrates are required to be cleaned thoroughly by washing in acetone followed by distilled water. Suitable deposition times are between one hour and two hours depending on the film thickness required. Following deposition, prepared structures are found to have further enhanced electrical properties if treated with a suitable chemical and annealed at elevated temperatures above 200°C in air or nitrogen atmosphere for 15 to 30 minutes. Annealing in this way is found to improve both the bulk properties of materials and electrical properties of the resultant devices.

Example 2

Fig. 5 schematically illustrates a second preferred embodiment of a multi-layer graded band gap photovoltaic device structure as configured in accordance with the present invention. The example given comprises an n-n-p (two junction) configuration 501. The device 501 comprises a glass substrate 502 coated with a conducting glass layer 503. Adjacent to layer 503 is window material layer 504 which may comprise n-type ZnSe, CdS or Cu_2O for example. Adjacent to window material layer 504 is a first (n-type) absorber layer 505 adjacent to which

is a further (p-type) absorber layer 506. Finally, adjacent to outer absorber layer 506 is configured a back electrical contact layer 507 which is ohmic to the p-type semi-conductor.

The energy band diagram for device 501 is given in Fig. 6 wherein at the junction between back contact layer 507 and outer absorber layer 506 there is formed an ohmic contact at 601. As was seen in the first example given above, the potential gradient, or the internal electric field of the device structure is again such that movement of electrons 602 is facilitated through the structure from outer absorber layer 506 to absorber layer 505 and then to window material 504. Similarly, movement of holes 603 is in the opposite direction. Suitably absorber layer 505 may comprise $CuInS_2$ and absorber layer 506 may comprise $CuInSe_2$.

Fig. 7 schematically illustrates the steps involved in fabricating a device of the type shown in Fig. 6. Steps 701 to 703 are substantially identical to steps 401 to 403 as described in relation to Fig. 4 earlier. Following step 703, at step 704 a first absorber layer is deposited and doped so as to change the composition of the layer appropriately and obtain an n-type semi-conductor material. A suitably configured material is, for example, n-type $CuInS_2$ or n-type In-rich $CuInGaSe_2$. Following deposition of a first absorber layer at step 704, at step 705 a second absorber layer is deposited and doped accordingly to obtain a p-type semi-conductor material. A suitable p-type semi-conductor material is, for example, Cu-rich $CuInSe_2$. Absorber layers 1 and 2 can be obtained from the same bath using different deposition voltages as will be understood by those skilled in the art. Following step 705, the resultant layers of the device are chemically treated and annealed, and the top surface is etched as indicated at step 706. Following step 706 an ohmic contact is formed to the p-type absorber layer 2 via metalisation, as indicated at step 707. One example of a complete device is:

Glass/CG/n-ZnSe/n-$CuInGaSe_2$/p-$CuInSe_2$/Ohmic metal contact

Example 3

Fig. 8 schematically illustrates a third preferred embodiment of a photovoltaic cell as configured in accordance with the present invention. Device

801 comprises an outer glass substrate layer 802 coated with a conducting glass layer 803. Adjacent to layer 803 is configured an n-type window material layer 804. Thereafter, three absorber layers are configured respectfully adjacent to one another as follows:

absorber layer 1 (close to n-type), 805;

absorber layer 2 (close to p-type), 806; and

absorber layer 3 (p-type), 807.

Adjacent to absorber layer 807 is configured a back electrical contact (ohmic to p-type) 808. Layers 803 and 808 may thereafter be connected to suitably configured terminals so that the device may be incorporated in a suitable circuit requiring electrical power generated through the photovoltaic effect.

Fig. 9 schematically illustrates the energy band diagram associated with device 801 described above. At the junction between sub-layer 807 and back electrical contact 808 is formed an ohmic contact as indicated at 901. Since the device illustrated in Figs. 8 and 9 is, compared with the devices of Figs. 2, 3, 5 and 6, comprised of more absorber layers with gradually reducing band gaps, the solar radiation is absorbed gradually from the higher energy end towards the lower energy end producing charge carriers without releasing heat energy into the device structure. In other words, the band gap for a given semiconductor layer reduces with increasing depth from the front transparent window layer. Thus, with increasing depth in the device progressively different portions of electromagnetic spectrum are absorbed by the device. This advantageous cooling effect together with the use of a major part of the electromagnetic radiation enhances the performance, efficiency and the lifetime of the device.

Fig. 10 schematically illustrates the steps involved in manufacturing a device of the type schematically illustrated in Figs. 8 and 9. Steps 1001 to 1003

are respectively substantially similar to steps 401 to 403 of Fig. 4. Following step 1003, at step 1004 a first absorber layer is deposited, the absorber layer being of an appropriate composition to obtain ~n-type semi-conductor material, such as ~n-$CuInGaSe_2$. After step 1004, a second absorber layer is deposited at step 1005 again having an appropriate composition in order to obtain the required semi-conductor material. In step 1005 the required semi-conductor material is approximately p-type (denoted ~p-type), such as ~p-$CuInGaSe_2$. Following step 1005, a third absorber layer is deposited at step 1006. The appropriate composition required for absorber layer 3 is that to obtain a p-type semi-conductor material such as p-$CuInGaSe_2$. Each of layers 1 to 3 can be obtained from the same electrodeposition bath by varying the deposition potential. The last layer can also be treated to obtain the required conductivity, if necessary. Following step 1006, at step 1007 the layers are annealed and the top surface chemically etched. Following step 1007, an ohmic contact is formed to the outer absorber layer via metalisation as is indicated at step 1008.

One example of a complete device of the type indicated in Figs. 8 and 9 is:

Glass/CG/n-ZnSe/~n-$CuInGaSe_2$/~p-$CuInGaSe_2$/p-$CuInGaSe_2$/Ohmic metal contact

Example 4

Fig. 11 schematically illustrates a fourth preferred embodiment of a multi-layer graded band gap photovoltaic device structure 1100 as configured in accordance with the present invention. The device illustrated is an example of a p-p-n layer device structure. The device comprises a glass substrate layer 1101 which is adjacent to a conducting glass layer 1102. Adjacent to conducting glass layer 1102 is a p-type window material layer 1103. Adjacent to window material layer 1103 there is configured a first absorber layer 1104 which is p-type followed by a second absorber layer 1105 which is n-type. Finally, adjacent to the outer (second) absorber layer there is a back contact layer 1106 which is ohmic to n-type.

In operation incident light, for example sunlight, is received through glass substrate layer 1101 whereafter the light passes respectively through layers 1102, 1103, 1104 and 1105. The received light thereafter causes a current to be generated in a circuit connected to conducting glass layer 1102 and back contact layer 1106.

It is believed that the device illustrated in Fig. 11 is unique, particularly because p-ZnSe is used as the starting point window material. Examples of suitable absorber layers are as follows:

- Absorber layer 1: p-type $CuInS_2$ (band gap ~1.5 eV); and
- Absorber layer 2: n-type $CuInGaSe_2$ (band gap ~1.1 eV)

Thus, one example of a structure of the type illustrated schematically in Fig. 11 is:

Glass/CG/p-ZnSe/p-$CuInS_2$/n-$CuInGaSe_2$/Ohmic contact

The energy band diagram for the device of Fig. 11 is schematically illustrated in Fig. 12. The energy diagram illustrates the band gaps within each layer and clearly shows that the band gap is largest in the window material layer 1103, next largest in absorber layer 1, 1104 and yet further reduced in absorber layer 2, 1105. Thus, there is a successive decrease in band gap value from layers 1103, 1104 to 1105. In other words, light of a greater energy is absorbed by window material layer 1103 than for absorber layer 1 and similarly the energy of the light absorbed by absorber layer 1 is larger than that for absorber layer 2. This results in a stepped band gap diagram wherein the steps aid movement of electrons 1201 from window material layer 1103 through absorber layer 1104 into absorber layer 1105 and finally to ohmic contact 1106. Similarly, holes 1202 effectively, like air bubbles in water, are encouraged to move up each subsequent energy step formed between each layer - holes are thereby encouraged to move from absorber layer 1105 to absorber layer 1104 and thereafter from absorber layer 1104 to window layer 1103 and thereafter to

conducting glass layer 1102. In this way an efficient production of electrical current is thereby generated from the device.

The energy band diagram shown in Fig. 12 comprises a substantially constant band gap value for each particular layer. However, the transition from one layer to the next causes a substantial change in the band gap which is represented graphically by the band gap upper limit curve 1203 and by the band gap lower limit curve 1204. Upper limit curve 1203 comprises a substantially horizontal line for each individual layer, but comprises a high gradient connecting portion between two given layers. For example, between window material layer 1103 and the first absorber layer 1104 there is a sharp decrease in band gap value which is generally indicated at 1105. There is a similarly sharp decrease between layers 1104 and 1105. As a partial mirror image to the upper limit curve 1203 there is lower limit curve 1204. Lower limit curve 1204 comprises a substantially lower energy for a given band gap of a given layer than portions of curve 1204 having a high gradient, i.e. those portions between the layers which represents graphically the transgression from one layer to the next. In terms of the lower level 1206 the band gap lower limit energy level gradually increases respectively from absorber layer 1105 to absorber layer 1104 to window material layer 1103. In this way the electrons may be considered to act like marbles falling down a slope and the holes may be considered to act like air bubbles rising in water. A simple graphical analogy between objects falling and rising through water is well known to those skilled in the art and is common in describing band gap diagrams of this type.

In the example shown, the band gap change from window material layer 1103 to absorber layer 1104 is greater than that from absorber layer 1104 to absorber layer 1105. The change, as shown, is due to both a substantial drop in the upper level 1203 and, to some extent, an equivalent, but smaller, decrease in the lower level 1204.

Fig. 13 illustrates schematically the steps involved in fabricating the device illustrated schematically in Figs. 11 and 12. At step 1301 a glass/conducting glass substrate is cleaned so as to remove grease from the surface. Following step 1301 a p-type ZnSe layer is deposited by electrodeposition on the substrate. Following step 1302, at step 1303 the ZnSe window layer is doped using a suitable chemical containing a Group I element or a Group V element to obtain optimum electrical conductivity for the window layer. Dopants can be added during the growth as described or during the post-growth annealing process. Following step 1303, at step 1304 absorber layers 1 and 2 are deposited successively using an electrochemical technique. Absorber layers 1 and 2 are deposited such that the band gap values vary from large to smaller for absorber layers 1 and 2 respectively. In this way a graded band gap device structure is obtained. As stated previously, examples of suitable materials are:

- Absorber layer 1: p-type $CuInS_2$ (band gap ~1.5 eV); and
- Absorber layer 2: n-type $CuInGaSe_2$ (band gap ~1.1 eV).

During deposition of each absorber layer, the particular layer being deposited may be doped so as to obtain optimum p-type and n-type conduction respectively. Optimum doping is achieved through varying the indium composition in the material or by introducing an extrinsic element during growth of the layer or during the post-annealing process. Following step 1304, at step 1305 the second absorber layer is chemically treated, annealed and etched so as to produce an ohmic back metal contact to complete the fabrication of the device. Such treatment is known to those skilled in the art and may include dipping the absorber layer in indium chloride solution, for example, so as to introduce chlorine ions into the material. As is also known to those skilled in the art, the optimum chemical treatment; annealing and etching conditions/chemical agents varies from material to material.

The invention comprises use of one step electrodeposition of $CuInSe_2$ based semiconductor materials such as $CuInS_2$, $CuInGaS_2$, $CuInSe_2$,

$CuInGaSe_2$, $CuInTe_2$ and $CuInGaTe_2$ to obtain both n-type and p-type semiconducting layers with varying band gaps. Optimization of conductivity has been obtained using changes in stoichometry as described, for example using In-rich for n-type and Cu-rich for p-type, or treatment of the layers with suitable n-type doping agents such as $InCl_3$ treatment followed by annealing. The aforementioned new designs of multi-layer graded band gap solar cell structures have been fabricated and typical values for efficiencies found in connection with the preferred embodiments of the solar cells described above are over 15%.

Advantages of utilizing the methods described in accordance with the present invention include a substantial reduction in the cost of photovoltaic solar cells through use of a low cost electroplating technique to grow and develop the solar energy materials. This technique enables the fabrication of solar cells of approximately 2 microns total thickness, instead of about 200 microns thickness as used in crystalline silicon solar cell fabrication. Reducing the cost of materials utilized in manufacture is clearly desirable.

The preferred embodiments of the present invention described above are designed to capture as large a part of the solar energy spectrum as possible whilst minimizing energy losses as heat energy in the devices. In respect of the four preferred embodiments of the present invention described above, the front of a photovoltaic cell begins with a large band gap window material which is positioned in front of several absorber material layers with decreasing band gaps the further that a given absorber layer is away from the window layer. Each interface between any two layers involved contributes to enhance the internal electric field forming a tandem solar cell. Suitable window materials used include n-type ZnSe, CdS, Cu_2O or, in relation to the fourth example, p-type ZnSe. In respect of the devices as configured in accordance with the present invention, annealing and natural aging processes are believed to increase intermixing at the hetero-junctions thus converting the device to a multi junction graded band gap device structure having a significantly greater number of different band gap layers than initially fabricated. The number of such layers resulting may potentially reach infinity, enhancing charge carrier collection during operation under

illumination. Inter-mixing at the interfaces during annealing of the material layers, in the preferred temperature range of 325-375°C, has been found to give increased efficiency as compared with published efficiency values using more conventional methods of photovoltaic cell fabrication.

To date, the inventors have produced high efficiency solar cells as described by stacking electrodeposited $CuIn(X)_2$ based semiconductor layers as described. For example solar cell parameters observed to date for the devices as configured in accordance with the present invention are: V_{oc} over 350 mV, J_{sc} = over 60 mA cm^{-2}, FF = 0.6 and conversion efficiencies over 15% under AM1.5 conditions (100 mW cm^{-2}), where V_{oc} = open circuit voltage; J_{sc} = short circuit current density and FF = Fill Factor. These high efficiency values, obtained using a one step low cost electrodeposition technique, are higher than published values using the more mainstream techniques described in the literature such as for example, in the paper by R. N. Bhattacharya et. al., J. Electrochemical Soc. Vol. 143, No. 3, (1996), P. 854, i.e. 14.1% efficiency using electrodeposition plus evaporation plus selenized copper-indium diselenide based device structures.

Fig. 14 summarizes, in the form of a table, possible devices as configured in accordance with the present invention and as described in Figs. 2 – 13. For each example identified in column 1401 each parameter of the device so configured is identified at columns 1402-1408 respectively as follows:

- 1402 - window material, n or p-type and possible materials;
- 1403 - window material dopant - group element possibilities for obtaining optimum electrical conductivity through layer;
- 1404 - absorber layer 1 - n-type or p-type;
- 1405 - absorber layer 2 - n-type or p-type;
- 1406 - absorber layer 3 - n-type or p-type;

- 1407 - back contact type; and
- 1408 - preferred treatment conditions (if any).

Devices of the type described above and configured in accordance with the present invention may be prepared as fully depleted devices so as to have the complete region to be photovoltaic active.

In addition to the annealing process, natural aging is also thought to produce intermixing at the material boundaries and hence smooth out the band gap steps between layers thereby enhancing charge carrier collection within the device. The devices configured with 3 or 4 layers in accordance with the present invention appear to become multi-layer graded band gap devices having higher efficiencies with age and through an increased number of active absorber layers effectively being formed.

In contrast to known methods of fabrication of copper-indium based photovoltaic devices the methods in accordance with the present invention include depositing the layers of such a photovoltaic device in a non-conventional order. Thus in accordance with an aspect of the present invention the window layer is deposited on a given substrate before any copper-indium based layers are deposited. This is in sharp contrast to known methods such as that disclosed in Canadian patent no. CA 2056609. Fabrication in this way enables different substrates to be used as compared with known methods and this aids higher efficiency photovoltaic devices to be realised. Upon the window layer of a device being made in accordance with the methods of the present invention is then deposited at least a first layer of a substantially copper-indium based material. Upon the first copper-indium based material there then may, in preferred embodiments of the present invention, be deposited a further layer of a substantially copper-indium based material. In fact additional substantially copper-indium based material layers may be deposited in turn, thus building up a multi-layered device comprising two or more copper-indium based absorber

layers . Each copper-indium based layer may comprise a different copper-indium based material as compared to an adjacent layer since preferably different materials are used that exhibit different size band gaps. Differing band gaps are clearly advantageous so as to absorb photons of different energies from the electromagnetic spectrum.

It will be apparent to those skilled in the art that the illustrative examples of devices described above exhibit a further aspect of the present invention as follows. In accordance with an aspect of the present invention there is also provided a method of fabricating a substantially copper-indium based thin film photovoltaic device of the type comprising a deposited n-type or p-type window layer of a semiconductor photon absorber material and at least a first deposited substantially coppier-indium based photon absorber layer located substantially adjacent to the window layer, the method comprising the step of:

doping said first photon absorber layer with a dopant of the same type, that is n-type or p-type, as said window layer.

This aspect of the present invention is summarised in Figure 14, wherein it is readily seen that for an n-type window layer the first photon absorber layer is, in accordance with an aspect of the present invention, doped with an n-type dopant to enhance n-type electrical activity in the first photon absorber layer.

Alternatively the selected window material may be selected as p-type and the first photon absorber layer is then, in accordance with this aspect of the present invention, assumed p-type and doped with a p-type dopant. This method results in a photovoltaic device having improved efficiency over known copper-indium based photovoltaic devices. Doping in the way described may be termed 'inverse doping' as compared with the existing methods known to those skilled in the art. Inverse doping of the kind described is opposite to what is usually performed in photovoltaic device fabrication. Known doping methods are based on an assumed p-n junction model for the window and first photon absorber

layer. Thus for a prior art substantially copper-indium based photovoltaic device, the main body of the device contains a copper-indium based material. If this material is assumed to be p-type then the assumed prior art model of what is the most sensible type of doping suggests a p-type dopant in the copper-indium layer so as to reduce the electrical resistance in the material. However the inventors of the present invention have observed that doping with a p-type dopant in these circumstances actually increases the series resistance of the fabricated devices resulting in a drastic reduction of the efficiency (mainly due to a loss in the fill factor). Thus in contrast to normal procedures the present invention concerns doping of the first deposited copper-indium based layer with a dopant of the same type, that is n-type or p-type, as the window layer.

Claims:

1. A method of fabricating a substantially copper-indium based thin film photovoltaic device, said method being characterised by comprising the steps of:

(a) using electrodeposition, depositing a front window layer of a semiconductor material on a suitably configured electrically conductive substrate;

(b) doping said window layer to obtain optimum electrical conductivity in said window layer; and following steps (a) and (b),

(c) successively and electrochemically depositing a plurality of adjacent copper-indium based semiconductor absorber layers on top of said semiconductor window layer wherein each said absorber layer has a different band gap energy value to an adjacent said absorber layer.

2. The method as claimed in claim 1, wherein said adjacent copper-indium based semiconductor absorber layers are selected from the set of compounds comprising:

copper-indium disulphide based compounds;

copper-indium diselenide based compounds; and

copper-indium ditelluride based compounds.

3. The method as claimed in claim 1 or claim 2, additionally comprising the step of:

treating the outer surface of said outer absorber layers to optimise the electrical properties of said outer semiconductor absorber layers.

4. The method as claimed in claim 3, wherein said treatment comprises chemically etching said outer semiconductor absorber layer.

5. The method as claimed in any of claims 1 to 4, additionally comprising the step of:

metalising the outer surface of said outer semiconductor absorber layer to form a back electrical contact so as to enable said device to be connectable to an electric circuit.

6. The method as claimed in any preceding claim, wherein said method comprises the additional step of annealing said semiconductor layers at a temperature in the temperature range 325-375°C.

7. The method as claimed in any preceding claim, wherein said window semiconductor layer comprises:

an n-type semiconductor material selected from the set comprising ZnSe, CdS and Cu_2O.

8. The method as claimed in any preceding claim, wherein said window dopant is selected from the set of dopants comprising:

Group III; and Group VII elements.

9. The method as claimed in any of claims 1 to 6, wherein said window layer comprises:

a p-type semiconductor material.

10. The method as claimed in any of claims 1 to 6 or 9, wherein said window layer comprises:

p-type ZnSe semiconductor material.

11. The method as claimed in claim 9 or claim 10, wherein said window semiconductor layer is doped with a dopant selected from the set of dopants comprising:

Group I; and Group V elements.

12. The method as claimed in any preceding claim, wherein said window layer has a greater band gap energy value than any of said plurality of absorber layers.

13. The method as claimed in any preceding claim, wherein the band gap energy value of said absorber layers decreases with increased distance of a given said layer away from said window layer.

14. The method as claimed in claim 1, wherein:

a first deposited absorber layer comprises an n-type semiconductor material; and

a second absorber layer deposited adjacent to said first absorber layer comprises an n-type semiconductor material.

15. The method as claimed in claim 1 or claim 14, wherein said device further comprises a back Schottky barrier metal contact layer adjacent to the outermost deposited absorber layer.

16. The method as claimed in claim 1, wherein:

a first said deposited absorber layer comprises an n-type semiconductor material; and

a second said absorber layer deposited adjacent to said first absorber layer comprises a p-type semiconductor material.

17. The method as claimed in claim 1, wherein:

first said deposited absorber layer comprises an n-type semiconductor material;

a second said deposited absorber layer adjacent to said first absorber layer comprises close to a p-type semiconductor material; and

an outer absorber layer adjacent to said second absorber layer comprises a p-type semiconductor material.

18. The method as claimed in claim 16 or claim 17, wherein said device comprises a back Ohmic type electrical contact layer adjacent to the outermost deposited p-type absorber layer.

19. The method as claimed in claim 1, wherein:

a first said deposited semiconductor absorber layer comprises a p-type semiconductor material; and

a second said deposited semiconductor absorber layer, adjacent to said first said absorber layer, comprises an n-type semiconductor material.

20. The method as claimed in claim 19, wherein said device further comprises:

a back Ohmic type electrical contact layer adjacent to said second said deposited n-type absorber layer.

21. A substantially copper-indium based thin film photovoltaic device, wherein said device is characterised in that it comprises:

an electrically conductive front substrate upon which is comprised an electrodeposited window layer of a doped semiconductor material; and

having been successively deposited on top of said deposited window layer, a plurality of electrochemically and adjacently deposited copper-indium based semiconductor absorber layers, wherein each said absorber layer has a different band gap energy value to an adjacent absorber layer.

22. A photovoltaic device as claimed in claim 21, wherein said adjacent copper-indium based semiconductor absorber layers comprise at least one compound from the set comprising:

copper-indium disulphide based compounds;

copper-indium diselenide based compounds; and

copper-indium ditelluride based compounds.

23. A photovoltaic device as claimed in claim 21 or claim 22, wherein the outer surface of each absorber layer has been treated by chemical treatment, annealing and etching to optimise the electrical properties of said outer semiconductor absorber layers.

24. A photovoltaic device as claimed in claim 23, wherein said outer absorber layer has been chemically treated and annealed using a doping agent to improve n-type conduction.

25. A photovoltaic device as claimed in any of claims 21 to 24, wherein said window layer comprises a material from the set comprising:

n-type ZnSe; n-type CdS; and n-type Cu_2O.

26. A photovoltaic device as claimed in any of claims 21 to 25, wherein said dopant comprises an element to improve n-type conduction, said element being selected from the set comprising:

Group III elements; and Group VII elements.

27. A photovoltaic device as claimed in claim 21, wherein said window material comprises a p-type semiconductor material.

28. A photovoltaic device as claimed in claim 21 or claim 27, wherein said window material comprises p-type ZnSe based material.

29. A photovoltaic device as claimed in any of claims 21, 27 or 28, wherein said window material is doped with an element to improve p-type conduction said element being selected from the set comprising:

Group I elements; and Group V elements.

30. A photvoltaic device as claimed in any of claims 21 to 29, wherein said window layer has a greater band gap energy value than the band gap value of any of said plurality of absorber layers.

31. A photvoltaic device as claimed in any of claims 21 to 30, wherein the band gap energy value of said absorber layers decreases with increased distance of a given said absorber layer away from said window layer.

32. A photovoltaic device as claimed in claim 21, wherein said first said deposited absorber layer, deposited adjacent to said window layer, comprises an n-type semiconductor material; and

a second absorber layer deposited adjacent to said first absorber layer comprises an n-type semiconductor material.

33. A photovoltaic device as claimed in claim 21 or 32, wherein said device further comprises a back Schottky barrier metal electrical contact layer adjacent to the outermost deposited absorber layer.

34. A photovoltaic device as claimed in claim 21, wherein:

a first said deposited absorber layer comprises an n-type semiconductor material; and

a second said absorber layer deposited adjacent to said first absorber layer comprises of p-type semiconductor material.

35. A photovoltaic device as claimed in claim 21, wherein:

the first said deposited absorber layer comprises an n-type semiconductor material;

a second said deposited absorber layer adjacent to said first absorber layer comprises a close to p-type semiconductor material; and

an outer absorber layer adjacent to said second absorber layer comprises a p-type semiconductor material.

36. A photovoltaic device as claimed in claim 34 or claim 35, wherein said device comprises a back Ohmic electrical contact layer adjacent to the outermost deposited p-type absorber layer.

37. A photovoltaic device as claimed in claim 21, wherein:

a first said deposited absorber layer comprises a p-type semiconductor material; and

a second said deposited absorber layer, adjacent to said first deposited absorber layer, comprises an n-type semiconductor material.

38. A photovoltaic device as claimed in claim 37, wherein said device comprises a back Ohmic electrical contact layer adjacent to said second said deposited n-type absorber layer.

39. A photovoltaic device as claimed in any of claims 21 to 36, wherein said device comprises n-type window material and during operation, conducts electric current in accordance with:

electrons move from said absorber layers to said window layer; and

holes move in the opposite direction to said electrons.

40. A photovoltaic device as claimed in claim 37 or claim 38, wherein said device conducts electrical current in accordance with:

electrons move in a direction towards an Ohmic contact from said window layer through said respective absorber layers, each said respective absorber layer having a smaller band gap than the last; and

holes move substantially in the opposite direction to said electrons.

41. A method of fabricating a substantially copper-indium based thin film photovoltaic device of the type comprising:

a deposited n-type or p-type window layer of a semiconductor photon absorber material; and

at least a first deposited substantially copper-indium based photon absorber layer located substantially adjacent to said window layer;

said method being characterised by comprising the step of:

doping said first photon absorber layer with a dopant of the same type, that is n-type or p-type, as said window layer.

42. The method as claimed in claim 41, wherein said selected window material is n-type and said first photon absorber layer is doped with an n-type dopant.

43. The method as claimed in claim 42, wherein said n-type window layer is doped with an n-type dopant.

44. The method as claimed in any of claims 41 to 43, wherein said window layer is doped with a group III or VII element.

45. The method as claimed in claim 41, wherein said selected window layer is n-type doped with a group IIII or VII element and said first absorber layer is n-type, said method additionally comprising the steps of:

depositing a second n-type substantially copper-indium based photon absorber layer adjacent to said first copper-indium based photon absorber layer; and

configuring a back electrical contact to said second photon absorber layer wherein said back contact constitutes an n-Shottky type barrier.

46. The method as claimed in claim 41, wherein said selected window layer is n-type doped with a group III or VII element and said first photon absorber layer is n-type, said method additionally comprising the steps of:

depositing a second substantially copper-indium based photon absorber layer adjacent to said first photon absorber layer said second photon absorber layer being substantially p-type; and

configuring a back electrical contact to said second photon absorber layer wherein said back contact constitutes a p-Ohmic type contact.

47. The method as claimed in claim 41, wherein said selected window layer is n-type doped with a group III or VII element and said first photon absorber layer is n-type, said method additionally comprising the steps of:

depositing a second substantially copper-indium based photon absorber layer adjacent to said first photon absorber layer, said second photon absorber layer being substantially p-type;

depositing a third substantially copper-indium based photon absorber layer adjacent to said second photon absorber layer, said third photon absorber layer being substantially p-type; and

configuring a back electrical contact to said third, that is the outer, photon absorber layer wherein said back contact constitutes a p-type Ohmic contact.

48. The method as claimed in claim 41, wherein said selected window material is p-type and said first photon absorber layer is doped with a p-type dopant.

49. The method as claimed in claim 48, wherein said p-type window layer is doped with a p-type dopant.

50. The method as claimed in any of claims 41, 48 or 49, wherein said window layer is doped with a group I or V element.

51. The method as claimed in claim 41, wherein said selected window layer is p-type doped with a group I or V element and said first photon absorber layer is p-type, said method additionally comprising the steps of:

depositing a second substantially copper-indium based photon absorber layer adjacent to said first photon absorber layer, said second photon absorber layer being substantially n-type; and

configuring a back electrical contact to said second photon absorber layer wherein said back contact constitutes an n-Ohmic type contact.

52. The method as claimed in any of claims 41 to 51, wherein said window layer is deposited on a substrate and said first deposited substantially copper-indium based photon absorber layer is then deposited on said window layer.

53. The method as claimed in claim 41, wherein following the deposition of said first substantially copper-indium based photon absorber layer there are successfully deposited further layers of substantially copper-indium based photon absorber materials.

54. The method as claimed in any of claims 41 to 54, wherein said deposition of said layers is by electrodeposition.

55. The method as claimed in claim 41, wherein the order of deposition of the layers is:

the window layer followed by said first deposited copper-indium based photon absorber layer followed, if applicable, by successive deposition thereafter of one or more further substantially copper-indium based photon absorber layers.

56. A substantially copper-indium based thin film photovoltaic device of the type comprising:

an n-type or p-type window layer of a semiconductor photon absorber material deposited on an electrically conductive substrate; and

at least a first deposited substantially copper-indium based photon absorber layer located substantially adjacent to said window layer;

said device being characterised in that:

said first photon absorber layer has been doped with a dopant of the same type, that is n-type or p-type, as said window layer.

57. A thin film photovoltaic device of the type claimed in claim 56, wherein said window layer has been deposited on a substrate and thereafter said first deposited substantially copper-indium based photon absorber layer has been deposited on said window layer.

58. A thin film photovoltaic device as claimed in claim 56, wherein the order of deposition of said layers is as follows:

the window layer followed by said first deposited copper-indium based photon absorber layer and then, if appropriate, on top of said first photon absorber layer successive deposition thereafter of one or more further copper-indium based photon absorber layers.

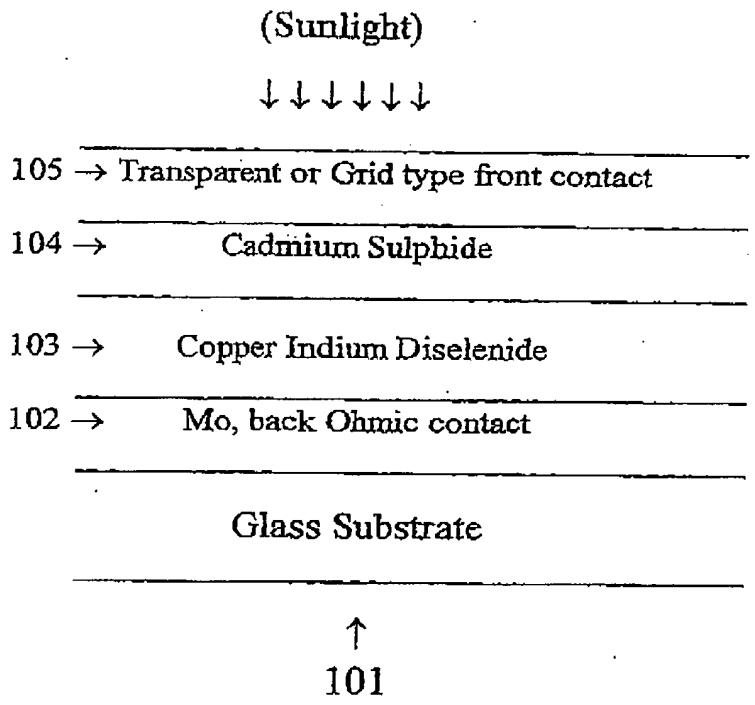

Figure 1
(Prior Art)

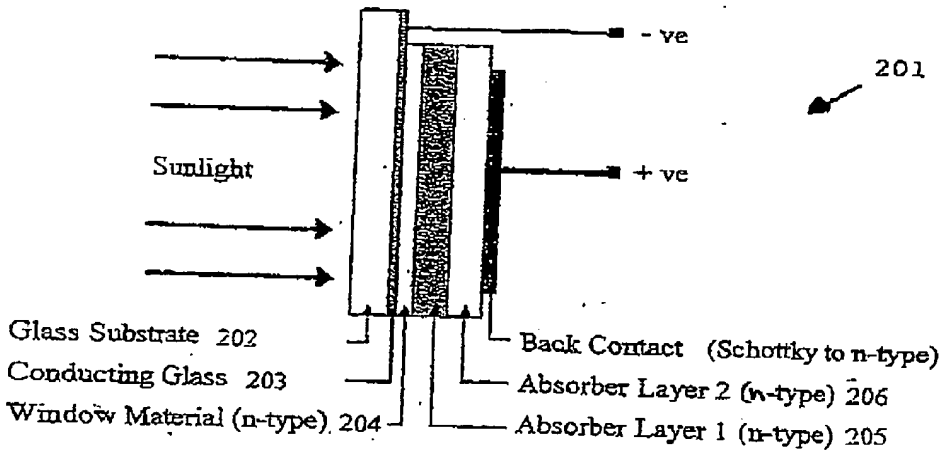

Fig.2. Schematic diagram of an example of an n-n-n layer device structure.

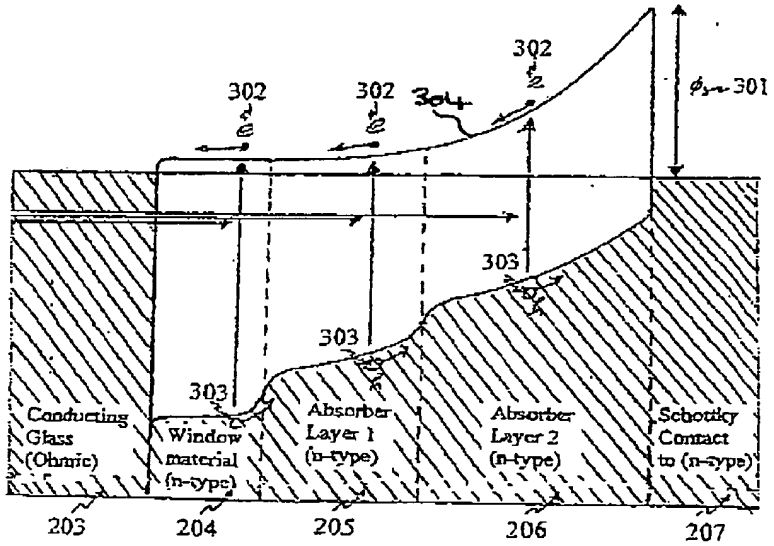

Fig.3. The energy band diagram of the device shown in fig. 2 (not to scale).

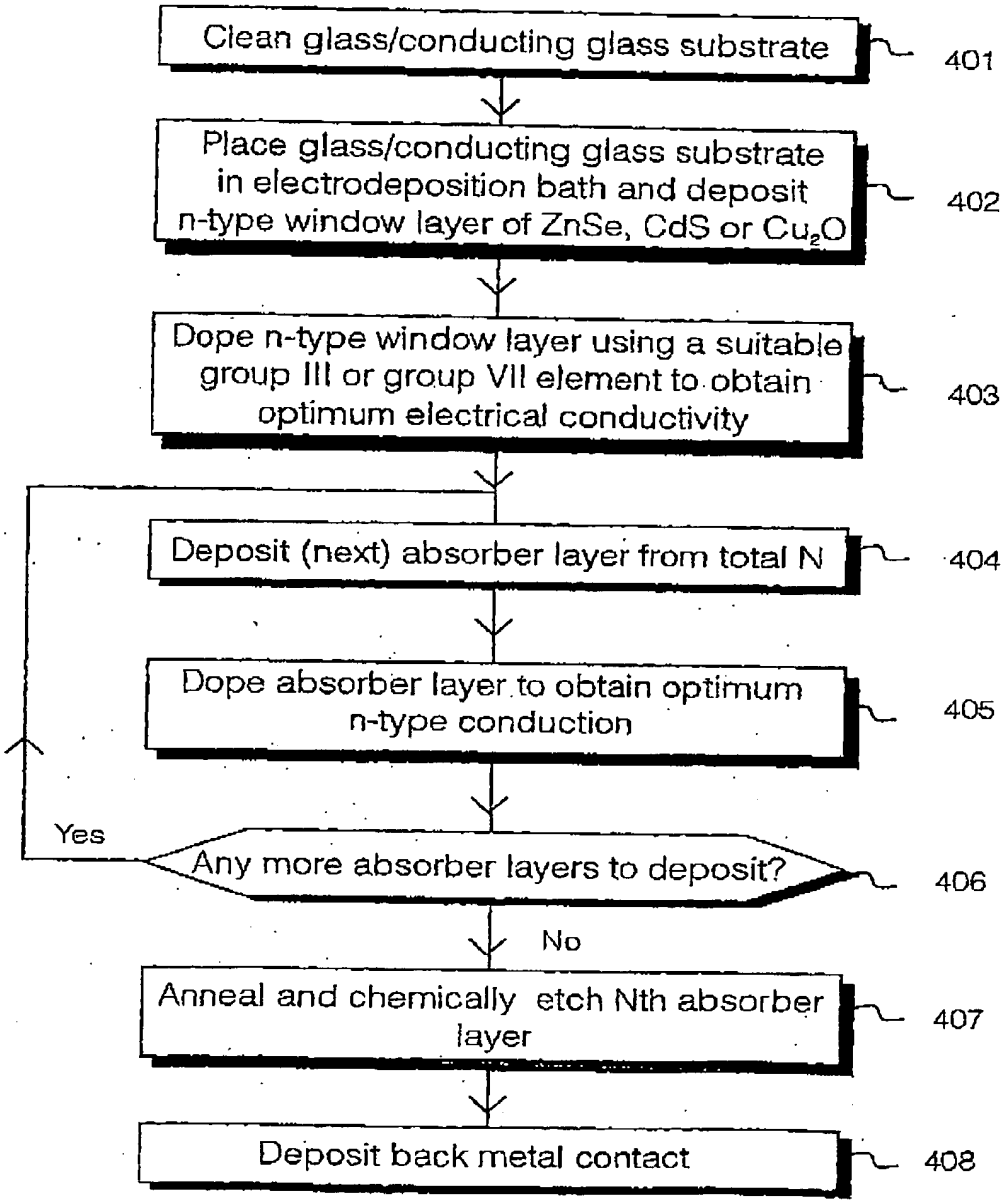
Clean glass/conducting glass substrate
401
Place glass/conducting glass substrate in electrodeposition bath and deposit n-type window layer of ZnSe, CdS or Cu_2O
402
Dope n-type window layer using a suitable group III or group VII element to obtain optimum electrical conductivity
403
Deposit (next) absorber layer from total N
404
Dope absorber layer to obtain optimum n-type conduction
405
Yes
Any more absorber layers to deposit?
406
No
Anneal and chemically etch Nth absorber layer
407
Deposit back metal contact
408

Fig. 4

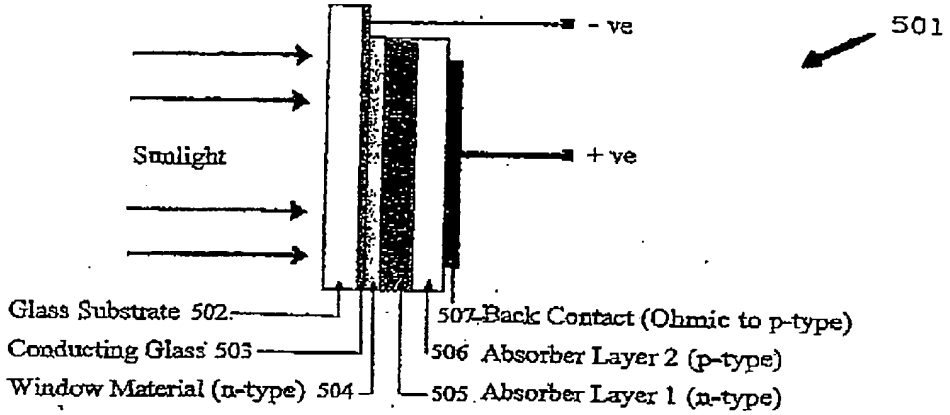

Fig.5. Schematic diagram of an example of an n-n-p layer device structure.

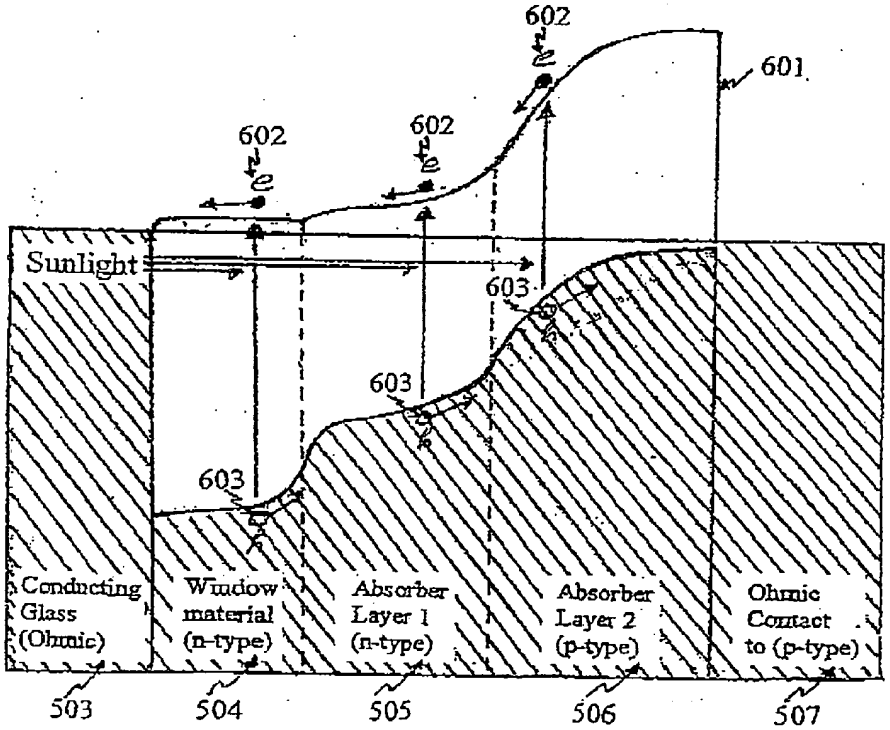

Fig.6. The energy band diagram of the device shown in fig. 5 (not to scale).

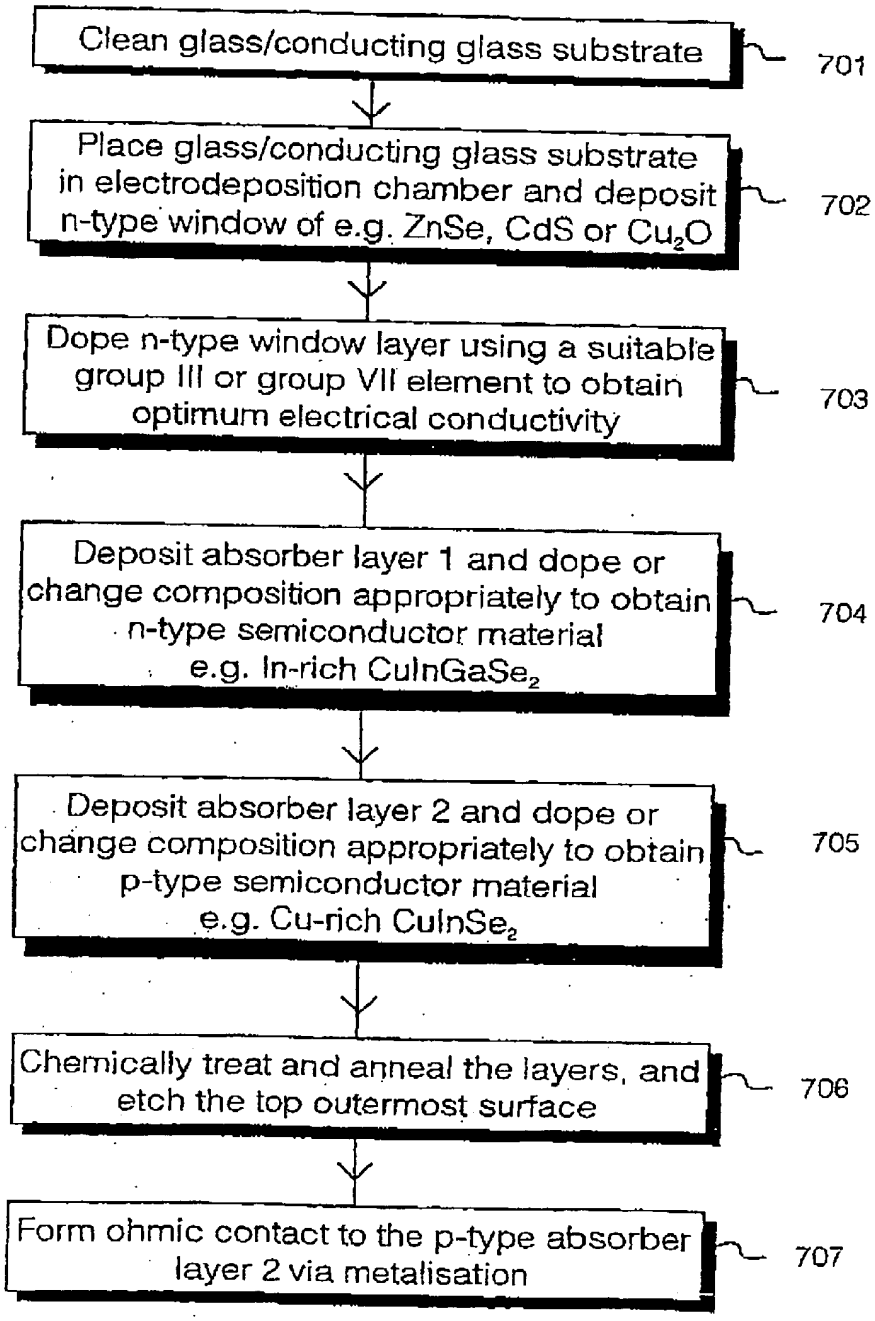
Clean glass/conducting glass substrate
701
Place glass/conducting glass substrate in electrodeposition chamber and deposit n-type window of e.g. ZnSe, CdS or Cu_2O
702
Dope n-type window layer using a suitable group III or group VII element to obtain optimum electrical conductivity
703
Deposit absorber layer 1 and dope or change composition appropriately to obtain n-type semiconductor material e.g. In-rich $CuInGaSe_2$
704
Deposit absorber layer 2 and dope or change composition appropriately to obtain p-type semiconductor material e.g. Cu-rich $CuInSe_2$
705
Chemically treat and anneal the layers, and etch the top outermost surface
706
Form ohmic contact to the p-type absorber layer 2 via metalisation
707

Fig. 7

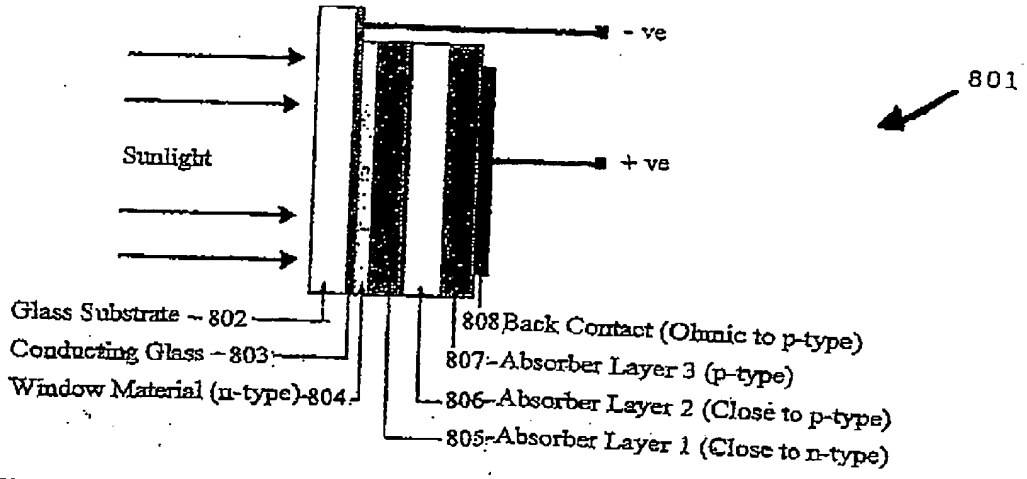

Fig.8. Schematic diagram of an example of an n-n-p-p- layer device structure.

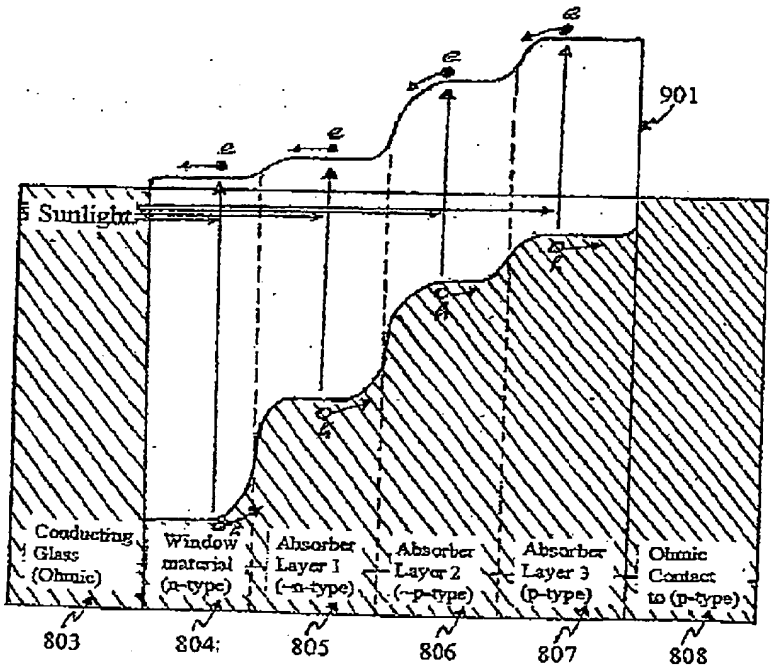

Fig. 9. The energy band diagram of the device shown in fig. 8 (not to scale)

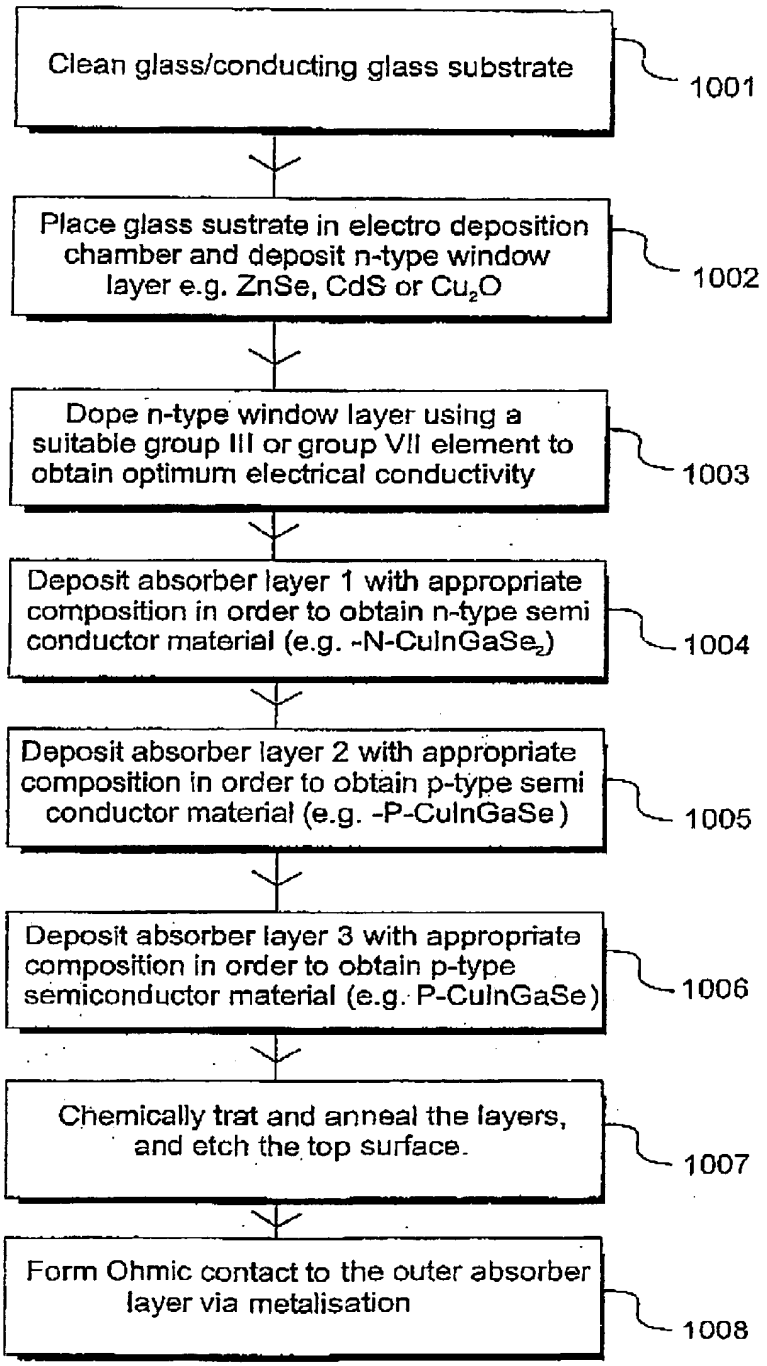
Clean glass/conducting glass substrate
1001
Place glass sustrate in electro deposition chamber and deposit n-type window layer e.g. ZnSe, CdS or Cu_2O
1002
Dope n-type window layer using a suitable group III or group VII element to obtain optimum electrical conductivity
1003
Deposit absorber layer 1 with appropriate composition in order to obtain n-type semi conductor material (e.g. -N-$CuInGaSe_2$)
1004
Deposit absorber layer 2 with appropriate composition in order to obtain p-type semi conductor material (e.g. -P-CuInGaSe)
1005
Deposit absorber layer 3 with appropriate composition in order to obtain p-type semiconductor material (e.g. P-CuInGaSe)
1006
Chemically trat and anneal the layers, and etch the top surface.
1007
Form Ohmic contact to the outer absorber layer via metalisation
1008

Fig.10

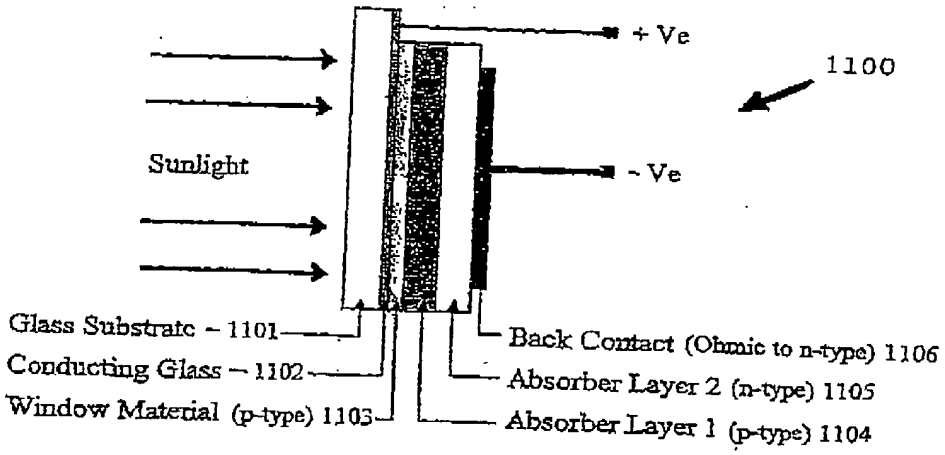

Fig.11. Schematic diagram of an example of a p-p-n layer device structure.

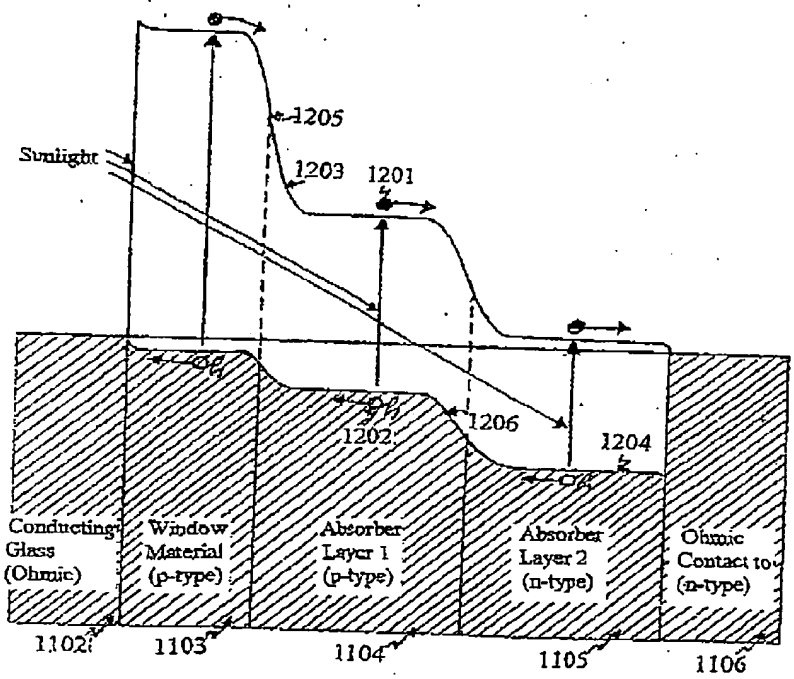

Fig.12. The energy band diagram of the device shown in fig.11 (not to scale).

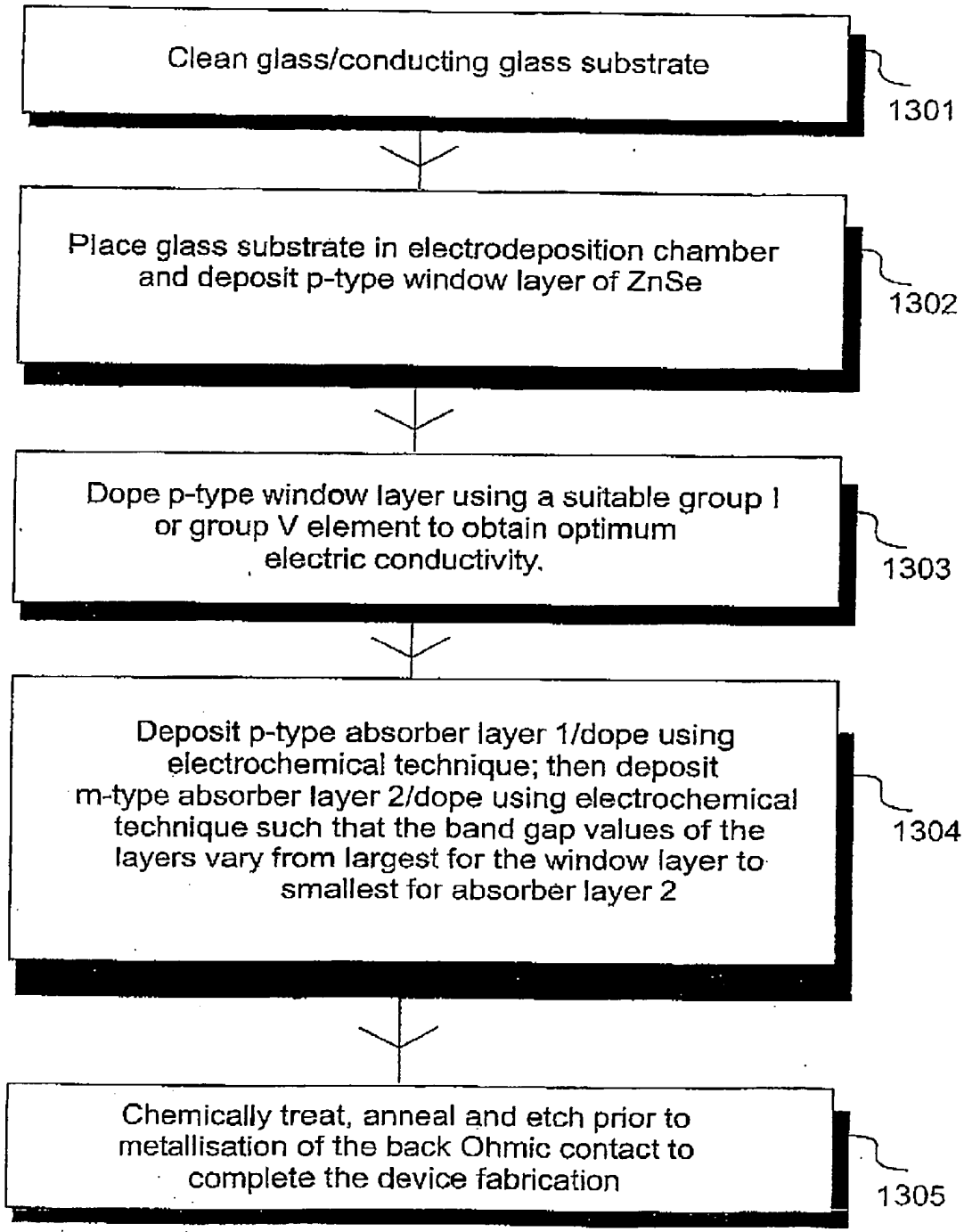
Clean glass/conducting glass substrate
1301
Place glass substrate in electrodeposition chamber and deposit p-type window layer of ZnSe
1302
Dope p-type window layer using a suitable group I or group V element to obtain optimum electric conductivity.
1303
Deposit p-type absorber layer 1/dope using electrochemical technique; then deposit m-type absorber layer 2/dope using electrochemical technique such that the band gap values of the layers vary from largest for the window layer to smallest for absorber layer 2
1304
Chemically treat, anneal and etch prior to metallisation of the back Ohmic contact to complete the device fabrication
1305

Fig.13

Example (1401)	Window (1402)	Window Dopant (1403)	Absorber Layer 1 (1404)	Absorber Layer 2 (1405)	Absorber Layer 3 (1406)	Back Contact (1407)	Treatment (1408)
I Figs 2-4	n-type ZnSe; CdS; or Cu^2O;	group III or VII Element	n-type	n-type	N/A	n-Schottky	Chemically treat, anneal, etch device as appropriate;
II Figs 5-7	n-type ZnSe; CdS; or Cu^2O;	group III or VII Element	n-type	p-type	N/A	p-Ohmic	Chemically treat, anneal, etch device as appropriate;
III Figs 8-10	n-type ZnSe; CdS; or Cu^2O;	group III or VII Element	n-type	p-type	p-type	p-Ohmic	Chemically treat, anneal, etch device as appropriate;
IV Figs11-13	p-type ZnSe;	group I or V Element	p-type (doped)	n-type (doped)	N/A	n-Ohmic	Chemically treat, anneal, etch device as appropriate;

Fig. 14

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0127113.9 10 November 2001 (10.11.2001) GB

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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20 November 2003

[Continued on next page]

(54) Title: COPPER-INDIUM BASED THIN FILM PHOTOVOLTAIC DEVICES AND METHODS OF MAKING THE SAME

Example (1401)	Window (1402)	Window Dopant (1403)	Absorber Layer 1 (1404)	Absorber Layer 2 (1405)	Absorber Layer 3 (1406)	Back Contact (1407)	Treatment (1408)
I Figs 2-4	n-type ZnSe; CdS; or Cu^IO;	group III or VII Element	n-type	n-type	N/A	n-Schottky	Chemically treat, anneal, etch device as appropriate;
II Figs 5-7	n-type ZnSe; CdS; or Cu^IO;	group III or VII Element	n-type	p-type	N/A	p-Ohmic	Chemically treat, anneal, etch device as appropriate;
III Figs 8-10	n-type ZnSe; CdS; or Cu^IO;	group III or VII Element	n-type	p-type	p-type	p-Ohmic	Chemically treat, anneal, etch device as appropriate;
IV Figs11-13	p-type ZnSe;	group I or V Element	p-type (doped)	n-type (doped)	N/A	n-Ohmic	Chemically treat, anneal, etch device as appropriate;

(57) Abstract: A method of fabricating a copper-indium based thin film photovoltaic device comprises the steps of: (a) using electrodeposition, depositing a front window layer of a semiconductor material on a suitably configured electrically conductive substrate: (b) doping the window layer to obtain optimum electrical conductivity in the window layer; and following steps (a) and (b), (c) successively electrochemically depositing a plurality of adjacent copper-indium based semiconductor absorber layers on the window layer wherein each absorber layer has a different band gap energy value to an adjacent absorber layer. Thus a copper-indium based thin film photovoltaic device made according to this method comprises; an electrically conductive front substrate upon which is comprised an electrodeposited window layer of a doped semiconductor material; and having been successively deposited on top of said deposited window layer, a plurality of electrochemically deposited adjacent copper-indium based semiconductor absorber layers, wherein each absorber layer has a different band gap energy value to an adjacent absorber layer.

WO 03/043096 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

PCT/GB 02/05058

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/0336 H01L31/032 H01L31/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DE 32 06 347 A (STANDARD ELEKTRIK LORENZ AG) 1 September 1983 (1983-09-01) page 4, lines 8-22; page 7, lines 7-20	1-40
Y	RAFFAELLE R P ET AL: "Scanning tunneling microscopy of electrodeposited CuInSe2 nanoscale multilayers" SOLAR ENERGY MATERIALS AND SOLAR CELLS, ELSEVIER SCIENCE PUBLISHERS, AMSTERDAM, NL, vol. 46, no. 3, 1 June 1997 (1997-06-01), pages 201-208, XP004084200 ISSN: 0927-0248 abstract; page 202, lines 11-29	1-40

-/—

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

* Special categories of cited documents :

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"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 August 2003	14/08/2003

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Wolff, G

INTERNATIONAL SEARCH REPORT

PCT/GB 02/05058

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 259 016 B1 (HAYASHI SHIGEO ET AL) 10 July 2001 (2001-07-10) column 5, line 3 -column 8, line 28; figures 1-3,5	41-58 16,34
Y	US 4 335 266 A (MICKELSEN REID A ET AL) 15 June 1982 (1982-06-15) column 10, line 4-67 column 13, line 59 -column 14, line 2 column 22, line 3-39; claims 1,40-42; figure 16; table I	5,14,15, 19,20, 32,33, 37,38
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Y	US 4 581 108 A (CHOUDARY UPPALA V ET AL) 8 April 1986 (1986-04-08) column 4, line 16 -column 6, line 65; figure 3	9-11, 27-29
Y	WO 98 48079 A (DAVIS JOSEPH & NEGLEY) 29 October 1998 (1998-10-29) page 9, line 19-24	6,24

INTERNATIONAL SEARCH REPORT

PCT/GB 02/05058

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

International Application No. PCT/GB 02 /05058

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-58

Device and method of manufacture of a substantially copper-indium based thin film photovoltaic device comprising an absorber layer adjacent to a window layer.

1.1. Claims: 1-40
device and method of manufacture of a substantially copper-indium based thin film photovoltaic device fabricated by electrodeposition and electrochemical deposition.

1.2. Claims: 41-58
Device and method of manufacture of a substantially copper-indium based thin film photovoltaic device wherein the photon absorber layer has the same doping type as the window layer.

Please note that all inventions mentioned under item 1, although not necessarily linked by a common inventive concept, could be searched without effort justifying an additional fee.

INTERNATIONAL SEARCH REPORT

PCT/GB 02/05058

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